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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/741,980	12/19/2000	Yasuhiro Teramoto	16869P015900	7969

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EXAMINER	
BAKER, PAUL A	

ART UNIT	PAPER NUMBER
2188	7

DATE MAILED: 10/23/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/741,980	Applicant(s) TERAMOTO, YASUHIRO	
	Examiner Paul A Baker	Art Unit 2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 December 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15,18,21,22 and 24* is/are rejected.

7)☒ Claim(s) *16,17,19,20 and 23* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on ~~*19 December 2000*~~ 11 June 2001 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *6* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Drawings

Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections

Claim 7 is objected to because of the following informalities: the claim does not end in a period. Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 9 recites the limitation "said comparing" in line 1. There is insufficient antecedent basis for this limitation in the claim. Claim 9 is considered to be dependent upon claim 8 for the purpose of examination.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-4, 6, 8-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Handy "The Cache Memory Handbook".

In regards to claim 1, Handy discloses a cache directory configuration, wherein each cache comprises a copy of a section of said main memory, said method comprising:

storing copies of address tags stored in said plurality of caches in a cache directory, wherein said cache directory is divided into a plurality of parts figure 2.8 "way a and b"; and

processing a plurality of search requests concurrently using said plurality of parts on page 54 2nd and 4th paragraphs.

In regards to claim 2, Handy discloses partitioning a search address tag associated with said search request into a plurality of sections;

responsive to said search request, determining if a first section of said plurality of sections matches an entry in a first part of said plurality of parts; and

when no match is indicated for any entry in said first part, returning a result on page 55 1st paragraph.

In regards to claim 3, Handy discloses when a match is indicated for any entry in said first part, determining if a second section of said plurality of sections matches an entry in a second part of said plurality of parts on page 55 1st paragraph each way is checked regardless whether another way has a match or not, therefore Handy checks the second section when a match is indicated in the first part.

In regards to claim 4, Handy discloses each entry in said cache directory is divided up into a plurality of entry groups; and each entry group can he operated on independently on page 54 paragraph 4.

In regards to claim 6, Handy discloses responsive to a search request of said plurality of search requests, determining if said search request matches any entry in a part of said plurality of parts; and when a match is indicated, returning a result on page 55 1st paragraph.

In regards to claim 8, Handy discloses a method for searching a cache directory comprising:

receiving a search request address tag;

partitioning said search request address tag into a first plurality of sections;

partitioning each address tag of said plurality of address tags into a second plurality of sections;

comparing for each address tag, a first section of said first plurality of sections with a first section of said second plurality of sections; and

returning a result when said comparing indicates no match for any address tag of said plurality of address tags on page 18 2nd paragraph.

In regards to claim 9, Handy discloses said comparing indicates a match for any address tag of said plurality of address tags, further comparing for each address tag, a second section of said first plurality of sections with a second section of said second plurality of sections on page 55 1st paragraph.

In regards to claim 10, Handy discloses a method for searching a cache directory used to maintain coherence between a cache and a main memory, comprising a plurality of memory banks, the cache directory comprising a plurality of sections in figure 2.8, the method comprising:

receiving a write request address by the cache directory to the main memory from another processor;

determining from the write request address a memory bank of the plurality of memory banks on page 54 4th paragraph;

selecting a section of the plurality of sections associated with the memory bank; and

searching the section for the write request address on page 55 1st paragraph.

In regards to claim 11, Handy discloses determining includes using a bit of the write request address on page 54 4th paragraph.

In regards to claim 12, Handy discloses the section comprises every other entry in the cache directory on page 55 1st paragraph.

Claims 1, 5, 7, 14, 15, 18 are rejected under 35 U.S.C. 102(b) as being anticipated by Gannon et al., US Patent 5,265,232.

In regards to claim 1, Gannon discloses a cache directory configuration method for maintaining coherence between a plurality of caches, wherein each cache comprises a copy of a section of said main memory, said method comprising:

storing copies of address tags stored in said plurality of caches in a cache directory in figure 10, wherein said cache directory is divided into a plurality of parts in figure 11 XI directory sections 0-R; and

processing a plurality of search requests concurrently using said plurality of parts in column 11 lines 41-43.

In regards to claim 5, Gannon discloses the plurality of parts comprises a first sub directory having even bits of each entry in the cache directory and a second sub directory having odd bits of each entry in the cache directory in column 11 line 44.

In regards to claim 7, Gannon discloses an information processing device comprising:

a plurality of processing devices, each of said plurality of processing devices comprising a cache storage module storing a copy of a section of a main storage device in figure 11 CPU 1-CPU N;

the main storage device shared by said plurality of processing devices and formed as a plurality of banks, wherein said banks having different address spaces and capable of operating in parallel figure 11 IRTLV 1-4; and

a coherence control device comprising a cache directory for providing coherence between a cache storage module and said main storage device figure 11 XI DIRECTORY SECTION 0-R, said cache directory storing copies of address tags associated with said cache storage module (figure 10), said cache directory being divided into a plurality of units capable of operating in parallel, and said coherence control device processing a plurality of search requests concurrently using said plurality of units figure 11 XI DIRECTORY SECTION 0-R.

In regards to claim 14, Gannon discloses a method for searching a cache directory used in maintaining coherence among caches in a multiprocessor system, comprising:

partitioning the cache directory into a plurality of parts, wherein each part of the plurality of parts is searched concurrently with another part of the plurality of parts figure 11 XI directory section 0-R;

partitioning a plurality of requests to the cache directory into a plurality of sub-requests, wherein each sub-request corresponds to a part of the plurality of parts; and searching in parallel, each part using an associated sub-request column 11 lines 41-62.

In regards to claim 15, Gannon discloses each part is associated with a memory bank of the multiprocessor system in figure 11 XI Directories 0-R is association with L2 Cache Sec 0-R.

In regards to claim 18, Gannon discloses a cache directory configuration system for maintaining coherence between a plurality of caches, wherein each cache comprises a copy of a section of said main memory, said system comprising:

a cache directory, comprising copies of address tags stored in said plurality of caches, wherein said cache directory is divided into a plurality of parts in figure 11 XI directories 0-R; and

a plurality of units for processing a plurality of search requests concurrently using said plurality of parts in column 11 lines 48-62.

In regards to claim 21, Gannon discloses each entry in said cache directory is divided up into a plurality of entry groups; and each entry group can be operated on independently in column 11 lines 50-54.

In regards to claim 22, Gannon discloses the plurality of parts comprises a first sub directory having even bits of each entry in the cache directory and a second sub directory having odd bits of each entry in the cache directory in column 11 line 44.

Claims 13 and 24 are rejected under 35 U.S.C. 102(e) as being anticipated by Bauman US Patent 6,480,927.

In regards to claim 13, Bauman discloses a system comprising a plurality of memory banks, in a multi-processor system, the cache directory comprising a plurality of sub-directories:

an input module for receiving a plurality of requests to the cache directory figure 10 element 1080;

a crossbar switch for coupling the input module with the plurality of sub-directories figure 5 element 530; and

a control module for routing a first request of the plurality of requests to a first subdirectory of the plurality of pub-directories and a second request of the plurality of requests to a second subdirectory of the plurality of sub-directories for concurrent searching of the first and second subdirectories, when the first and second requests

address different memory banks of the plurality of memory banks figure 10 element 1040 in communication with figure 5 element 530 to transfer data to figure 6 sub-directories 630A-D.

In regards to claim 24, Bauman discloses a system comprising a plurality of memory banks, in a multi-processor system, the cache directory, comprising a plurality of sections, the system comprising:

an input module for receiving a write request address by the cache directory from another processor figure 10 element 1080;

a bank selector module for determining from the write request address, a memory bank of the plurality of memory banks figure 10 element 1040;

a switch for selecting a section of the plurality of sections associated with the memory bank figure 5 element 530; and

a comparison module for searching the section for the write request address figure 12 element 1230.

Allowable Subject Matter

Claims 16-17,19-20, and 23 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Hayes et al. US Patents 5,909,697 and 6,073,212 disclose using dual tag directories for storing information.

Chang et al., US Patent 6,311,253 discloses a means for partial cache directory entries.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul A Baker whose telephone number is (703)305-3304. The examiner can normally be reached on M-F 10am-6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (703)306-2903. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)305-3900.

PB

Mano Padmanabhan
10/10/03

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